

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Currently Amended) A digital signal processing system,  
2 comprising:

3 a plurality of processor subsystems that each include:  
4 at least one memory device; and  
5 a memory bus multiplexer coupled to each of said at  
6 least one memory device by a subsystem memory bus;  
7 and  
8 a direct memory access (DMA) controller,  
9 wherein each of the DMA controllers is coupled to each of said  
10 memory bus multiplexers of each of said plurality of  
11 processor subsystems and is configured to access each of  
12 said memory devices of each of said plurality of  
13 processor subsystems via the corresponding subsystem  
14 memory bus.

2. (Canceled)

1 3. (Currently Amended) The system of claim 1, wherein each of the  
2 plurality of processor subsystems further includes:

3 a host port interface (HPI) unit coupled to the memory  
4 bus multiplexer and configured to access the memory  
5 device via the subsystem memory bus; and  
6 wherein each of the HPI units is coupled to each of the memory  
7 bus multiplexers of each of said plurality of processor  
8 subsystems and is configured to access each of the memory  
9 devices of each of said plurality of processor subsystems  
10 via the corresponding subsystem memory bus.

4. (Canceled)

1 5. (Currently Amended) The A digital signal processing system, of  
2 ~~claim 1~~, wherein ~~each of the plurality of processor subsystems~~  
3 ~~further includes comprising~~:

4 a plurality of processor subsystems that each include:

5 at least one memory device; and

6 a memory bus multiplexer coupled to each of said at  
7 least one memory device by a subsystem memory bus;  
8 and

9 a direct memory access (DMA) controller,

10 an input/output peripheral coupled to the subsystem  
11 memory bus,

12 wherein each of the DMA controllers is coupled to each of said  
13 memory bus multiplexers of each of said plurality of  
14 processor subsystems and is configured to access each of  
15 said memory devices of each of said plurality of  
16 processor subsystems via the corresponding subsystem  
17 memory bus, and

18 wherein each of the DMA controllers is configured to access  
19 each of the peripherals via the corresponding subsystem  
20 memory bus.

1 6. (Currently Amended) The A digital signal processing system, of  
2 ~~claim 4~~, wherein ~~each of the plurality of processor subsystems~~  
3 ~~further includes comprising~~:

4 a plurality of processor subsystems that each include:

5 at least one memory device; and

6 a memory bus multiplexer coupled to each of said at  
7 least one memory device by a subsystem memory bus;  
8 and

9 a direct memory access (DMA) controller,

10        a host port interface (HPI) unit coupled to the memory  
11            bus multiplexer and configured to access the memory  
12            device via the subsystem memory bus; and  
13        a remote access multiplexer coupled between the memory  
14            bus multiplexer and all DMA controllers outside the  
15            processor subsystem, wherein the remote access  
16            multiplexer is further coupled between the memory  
17            bus multiplexer and all HPI units outside the  
18            processor subsystem,  
19        wherein each of the DMA controllers is coupled to each of said  
20            memory bus multiplexers of each of said plurality of  
21            processor subsystems and is configured to access each of  
22            said memory devices of each of said plurality of  
23            processor subsystems via the corresponding subsystem  
24            memory bus;  
25        wherein each of the HPI units is coupled to each of the memory  
26            bus multiplexers and is configured to access each of the  
27            memory devices via the corresponding subsystem memory bus  
28            wherein each of the HPI units is coupled to each of the  
29            memory bus multiplexers and is configured to access each  
30            of the memory devices via the corresponding subsystem  
31            memory bus; and  
32        wherein the memory bus multiplexer is configured to couple to  
33            the memory bus at any one time exactly one of the HPI  
34            unit, the DMA controller, and the remote access  
35            multiplexer.

1    7. (Original) The system of claim 6, wherein each of the plurality  
2    of processor subsystems further includes:

3        a remote access arbiter coupled to the remote access  
4            multiplexer and configured to set the remote access  
5            multiplexer to couple to the memory bus multiplexer at

6 any one time exactly one of the HPI units and DMA  
7 controllers outside the processor subsystem.

1 8. (Original) The system of claim 6, wherein each of the plurality  
2 of processor subsystems further includes:

3 a memory bus arbiter coupled to the memory bus multiplexer to  
4 arbitrate between access requests received from the HPI  
5 unit, the DMA controller, and the remote access  
6 multiplexer, wherein said arbitration is performed on a  
7 round-robin basis.

9. (Canceled)

1 10. (Currently Amended) A digital signal processor chip,  
2 comprising:

3 a plurality of memory bus multiplexers, each of the memory bus  
4 multiplexers is coupled to one or more corresponding  
5 memory devices by a corresponding memory bus; and

6 a plurality of DMA controllers each coupled to each of the  
7 plurality of memory bus multiplexers, each of the DMA  
8 controllers is configurable to access each of the memory  
9 devices via a corresponding one of the plurality of  
10 memory bus multiplexers;

11 a plurality of memory bus arbiters each coupled to a  
12 respective memory bus multiplexer, wherein each of the  
13 plurality of memory bus arbiters is configured to set  
14 their respective memory bus multiplexers to grant access  
15 to the corresponding memory bus in response to one or  
16 more access requests from the plurality of DMA  
17 controllers;

18 a plurality of host port interface (HPI) units each coupled to  
19 each of the plurality of memory bus multiplexers, and

20           each configured to access each of the memory devices via  
21           a corresponding one of the plurality of memory bus  
22           multiplexers; and  
23       a plurality of memory bus arbiters each coupled to a  
24           respective memory bus multiplexer, and each configured to  
25           arbitrate between a local DMA controller, a local HPI  
26           unit, and a remote access multiplexer for access to a  
27           memory bus.

11 and 12. (Canceled)

1 13. (Currently Amended) The chip of claim ~~11~~ 10, further comprising  
2 a plurality of memory bus arbiters each coupled to a respective  
3 memory bus multiplexer, wherein each of the plurality of memory bus  
4 arbiters is configured to set their respective memory bus  
5 multiplexers to grant access to the corresponding memory bus in  
6 response to one or more access requests from the plurality of DMA  
7 controllers.

1 14. (Original) The chip of claim 13, wherein the arbiters are  
2 further configured to resolve conflicts on a round-robin priority  
3 basis and grant only one access request at a time.

15 and 16. (Canceled)

1 17. (Original) A multi-core digital signal processor, comprising:  
2       a first processor subsystem that includes:  
3           a first processor core;  
4           a first memory device coupled to the first processor  
5           core by a first instruction bus;  
6           a first memory bus multiplexer coupled to the first  
7           memory device by a first memory bus;

8           a first DMA controller coupled to the first memory bus  
9           multiplexer and configured to control the first  
10          memory bus to access the first memory device;  
11          a first HPI unit coupled to the first memory bus  
12          multiplexer and configured to control the first  
13          memory bus to access the first memory device; and  
14          a first remote access multiplexer coupled to the first  
15          memory bus multiplexer; and  
16      a second processor subsystem that includes:  
17          a second processor core;  
18          a second memory device coupled to the second processor  
19          core by a second instruction bus;  
20          a second memory bus multiplexer coupled to the second  
21          memory device by a second memory bus;  
22          a second DMA controller coupled to the second memory bus  
23          multiplexer and configured to control the second  
24          memory bus to access the second memory device;  
25          a second HPI unit coupled to the second memory bus  
26          multiplexer and configured to control the second  
27          memory bus to access the second memory device; and  
28          a second remote access multiplexer coupled to the second  
29          memory bus multiplexer,  
30      wherein the first DMA controller is coupled to the second  
31      remote access multiplexer and is configured to control  
32      the second memory bus to access the second memory device,  
33      and  
34      wherein the second DMA controller is coupled to the first  
35      remote access multiplexer and is configured to control  
36      the first memory bus to access the first memory device.

1    18. (Original) The processor of claim 17, wherein the first HPI  
2    unit is coupled to the second remote access multiplexer and is

3 configured to control the second memory bus to access the second  
4 memory device, and wherein the second HPI unit is coupled to the  
5 first remote access multiplexer and is configured to control the  
6 first memory bus to access the first memory device.

1 19. (Original) The processor of claim 17, further comprising a  
2 first arbiter coupled to the first memory bus multiplexer and  
3 configured to arbitrate between the first DMA controller, the first  
4 HPI unit, and the first remote access multiplexer for control of  
5 the first memory bus.